What we claim is:

1. A method for testing bit errors comprising the steps of:

converting a testing serial signal into parallel signals corresponding to channels for a plurality of measured devices and a redundant channel to be demultiplexed for the measured devices;

converting a passing signal through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

multiplexing output signals of the measured devices and the channel determination signal corresponding to a demultiplexing mode; and

measuring bit errors from the multiplexed signals and detecting measured devices concerning the bit errors from the channel determination signal.

2. The method for testing bit errors as claimed in claim 1 wherein the channel determination signal comprises a signal in which all bits of the passing signal of the redundant channel are inverted.

3. The method for testing bit errors as claimed in claim 1 wherein the testing signal has a pseudo random pattern.

4. A device for testing bit errors comprising:

a signal generator for generating a testing serial signal;

a signal demultiplexer for converting the serial signal into parallel signals corresponding to channels for a plurality of measured devices and a redundant channel to be demultiplexed for the measured devices;

a channel determination signal generating circuit for converting a passing signal through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

a signal multiplexer for multiplexing output signals of the measured devices and the channel determination signal corresponding

to a demultiplexing mode of the signal demultiplexer; and

a bit error measuring device for measuring bit errors from output signals of the signal multiplexer and detecting measured devices concerning the bit errors from the channel determination signal.

5. The device for testing bit errors as claimed in claim 4 wherein the channel determination signal comprises a signal in which all bits of the passing signal of the redundant channel are inverted.

6. The method for testing bit errors as claimed in claim 2 wherein the testing signal has a pseudo random pattern.